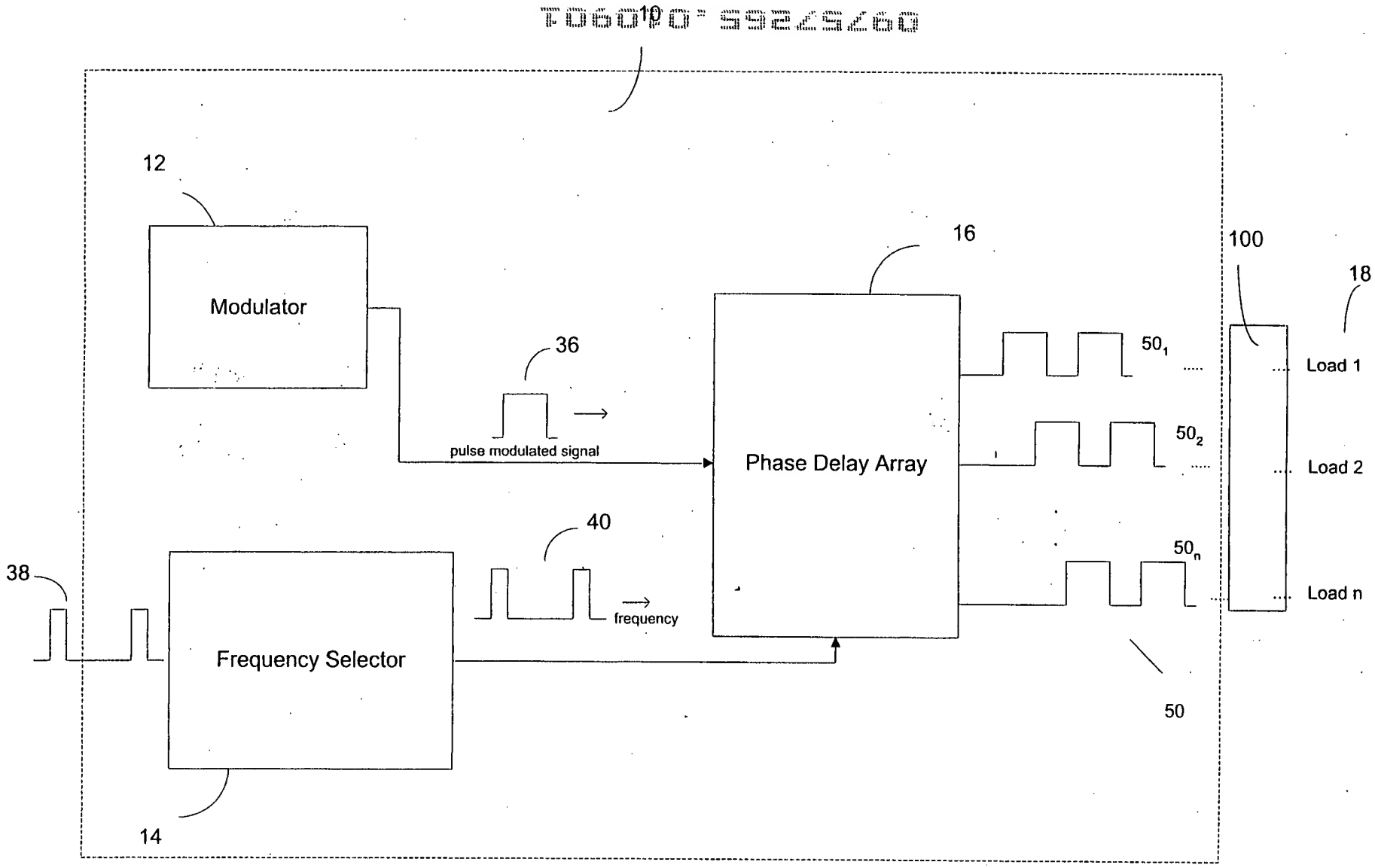

10
12
Modulator
16
100
18
36
pulse modulated signal
Phase Delay Array
50_1
Load 1
50_2
Load 2
40
50_n
38
frequency
Load n
Frequency Selector
50
14

FIGURE 1

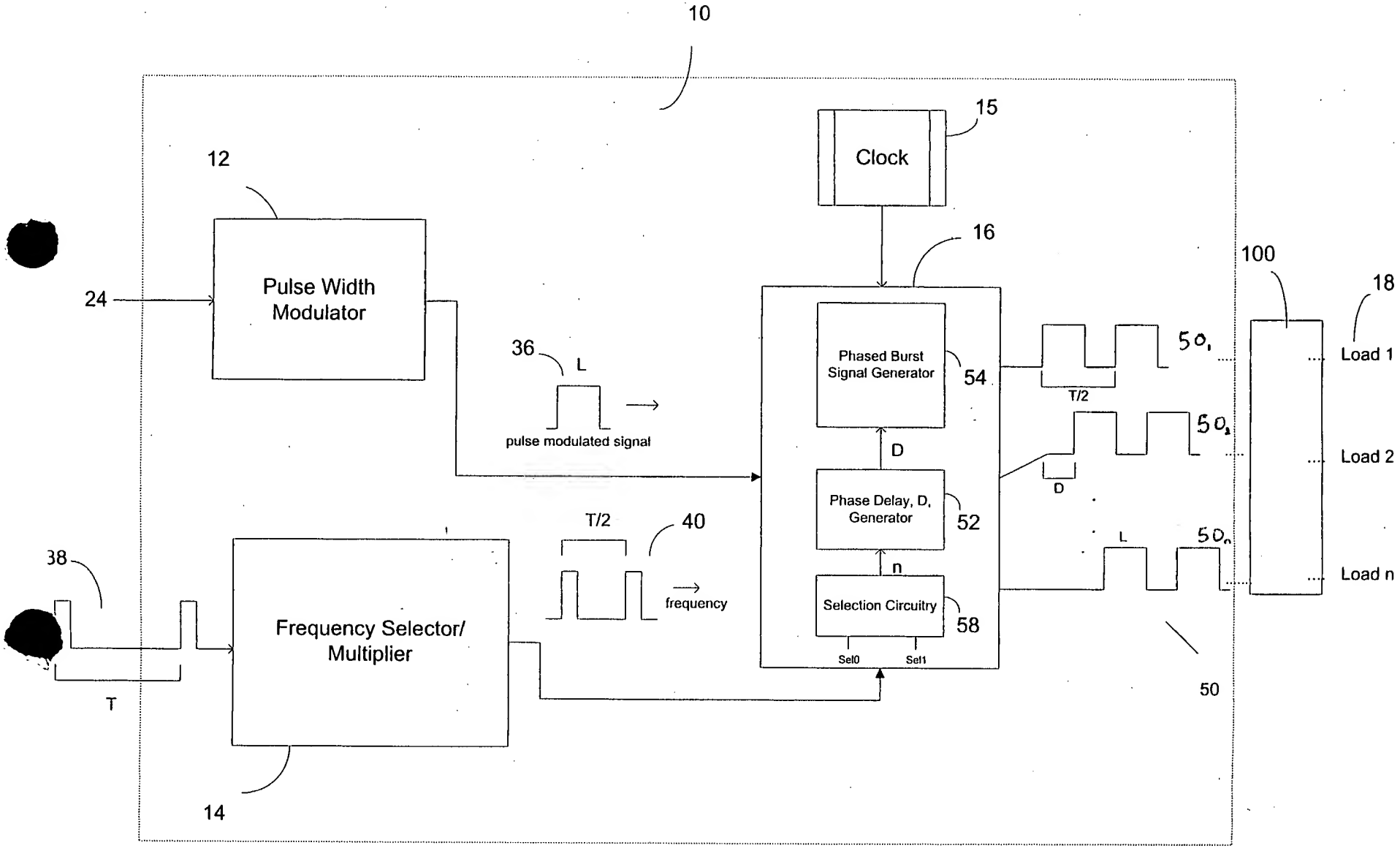

10
12
Pulse Width Modulator
24
15
Clock
16
36
L
pulse modulated signal
Phased Burst Signal Generator
54
D
Phase Delay, D, Generator
52
n
Selection Circuitry
58
Sel0
Sel1
T/2
40
frequency
38
T
Frequency Selector/ Multiplier
14
50
50₁
50₂
50n
T/2
D
L
100
18
Load 1
Load 2
Load n

FIGURE 2

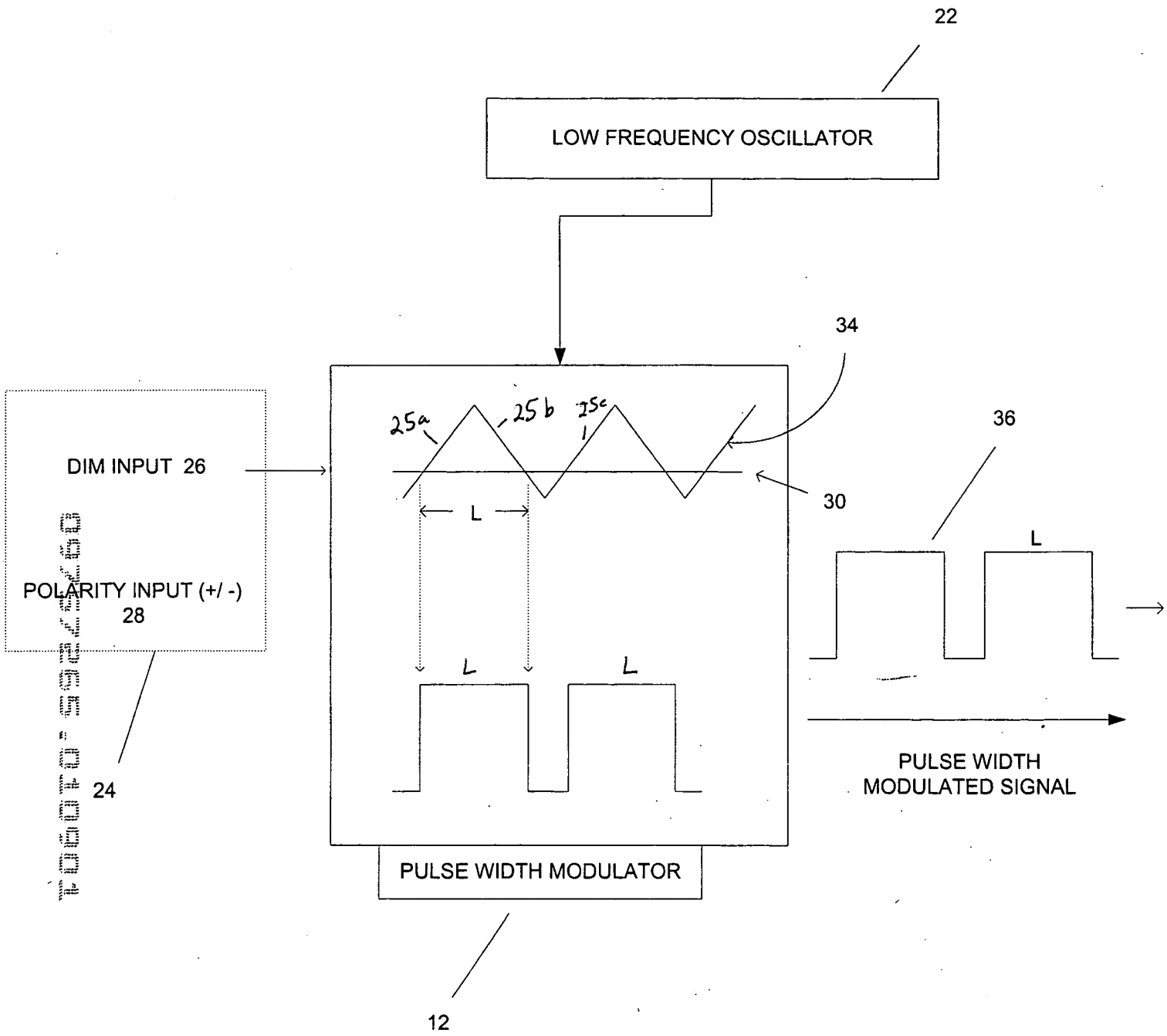

22
LOW FREQUENCY OSCILLATOR
34
25a
25b
25c
DIM INPUT 26
30
36
L
POLARITY INPUT (+/ -)
28
L
L
24
PULSE WIDTH
MODULATED SIGNAL
PULSE WIDTH MODULATOR
12

FIGURE 3

Best Available Copy

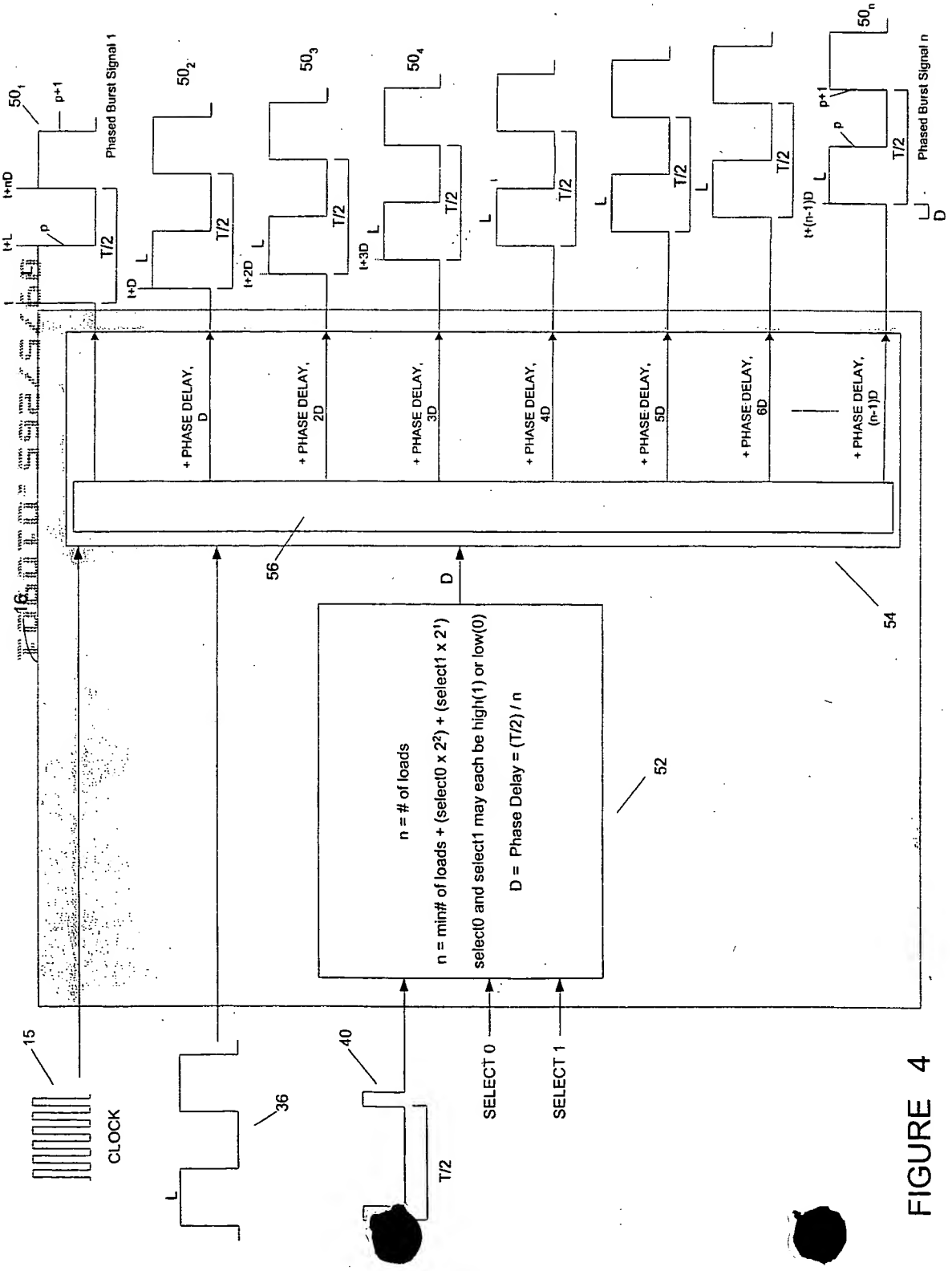


FIGURE 4

Sel0 (Select 0)	0	0	1	1
Sel1 (Select 1)	0	1	0	1
n (# of CCFLs)	6 (or min #)	8 (min # + 2)	10 (min# + 2^2)	12 (min#+2+2^2)

FIGURE 5 (a)

Sel0	0	1	0	1	0	1	0	1
Sel1	0	0	1	1	0	0	1	1
Sel2	0	0	0	0	1	1	1	1
n (# of loads)	min + 0	min + 2	min + 4	min + 6	min + 8	min + 10	min + 12	min + 14

FIGURE 5 (b)

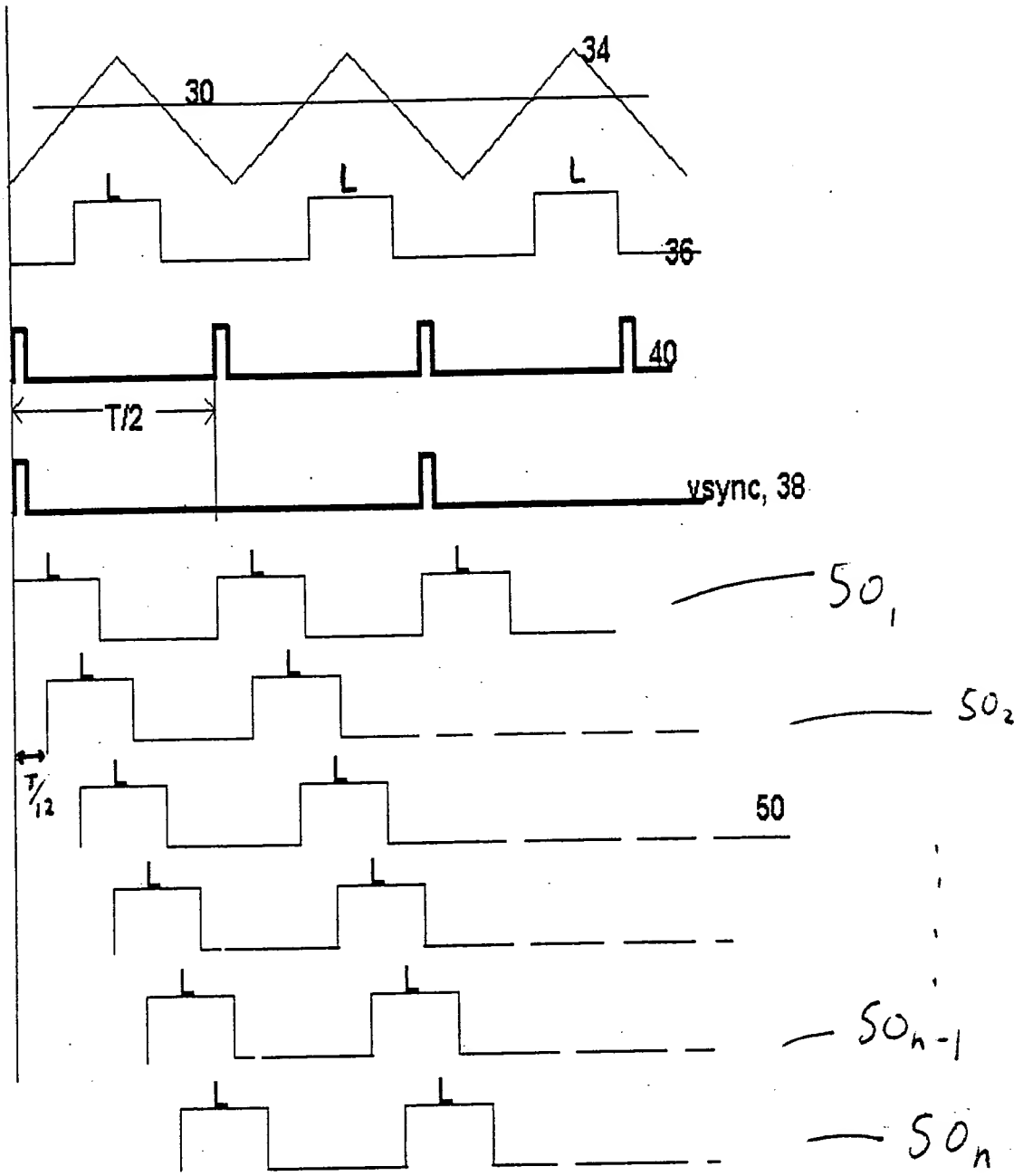


FIGURE 6

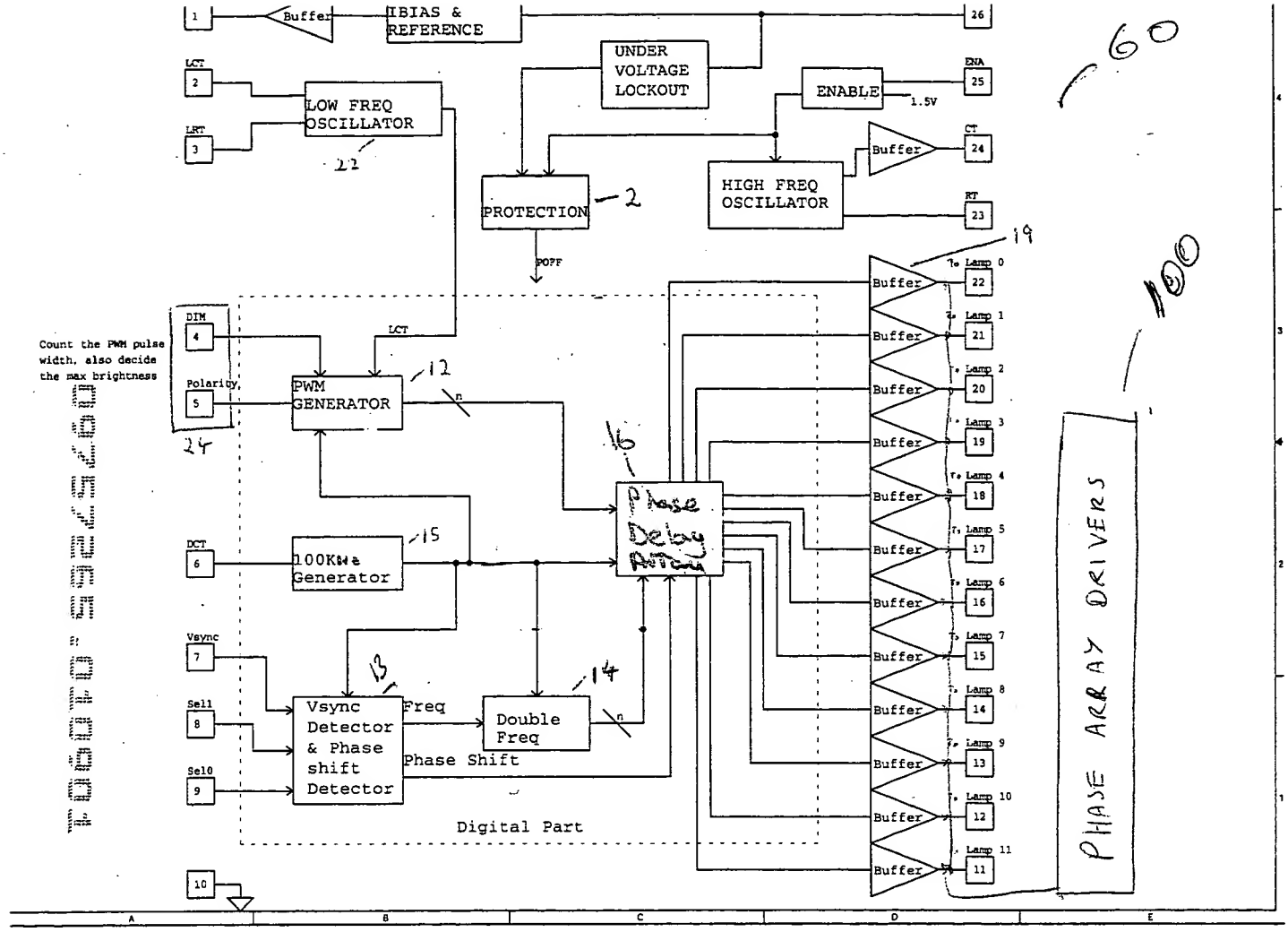

1
Buffer
IBIAS & REFERENCE
26
LCT
2
LOW FREQ OSCILLATOR
22
LRT
3
UNDER VOLTAGE LOCKOUT
ENABLE
1.5V
ENA
25
CT
24
Buffer
HIGH FREQ OSCILLATOR
RT
23
PROTECTION
2
POFF
19
160
100
Count the PWM pulse width, also decide the max brightness
DIM
4
Polarity
5
24
LCT
PWM GENERATOR
12
n
16
Phase Delay Adjust
DCT
6
100KHz Generator
15
Vsync
7
Sel1
8
Sel0
9
13
Vsync Detector & Phase shift Detector
Freq
Phase Shift
14
Double Freq
n
Digital Part
10
Buffer
Lamp 0
22
Lamp 1
21
Lamp 2
20
Lamp 3
19
Lamp 4
18
Lamp 5
17
Lamp 6
16
Lamp 7
15
Lamp 8
14
Lamp 9
13
Lamp 10
12
Lamp 11
11
PHASE ARRAY DRIVERS
A
B
C
D
E

FIGURE 7

TOSOTO 99259260

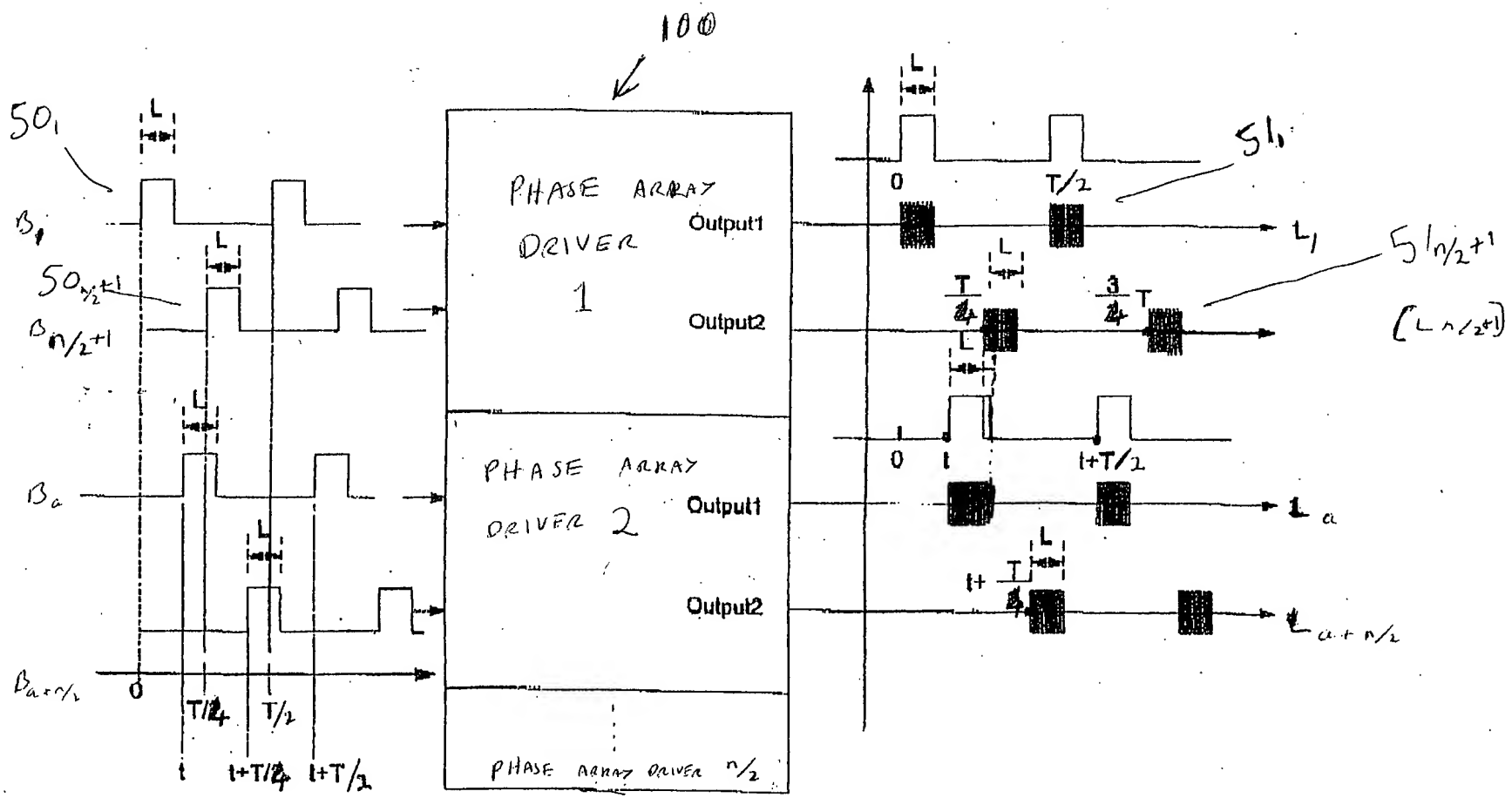


FIGURE 8

TD6070-S82S260

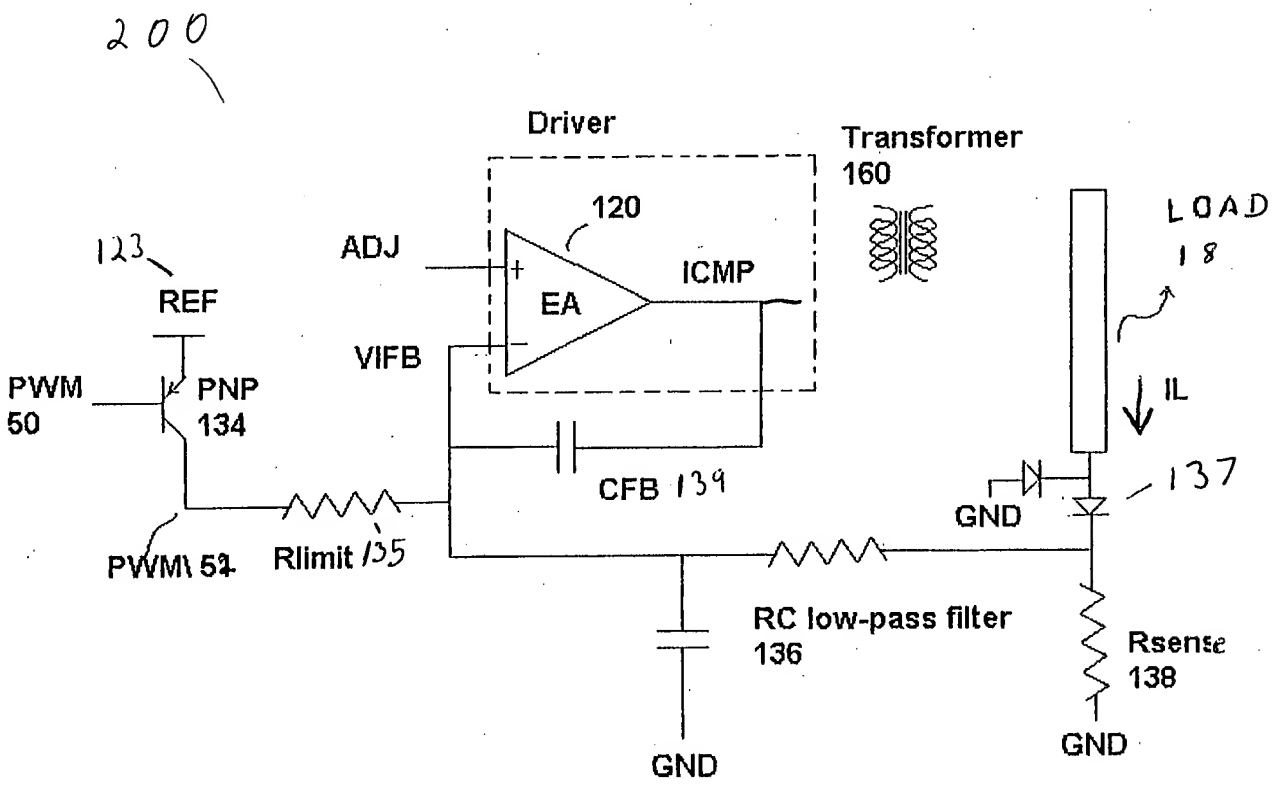


FIGURE 9

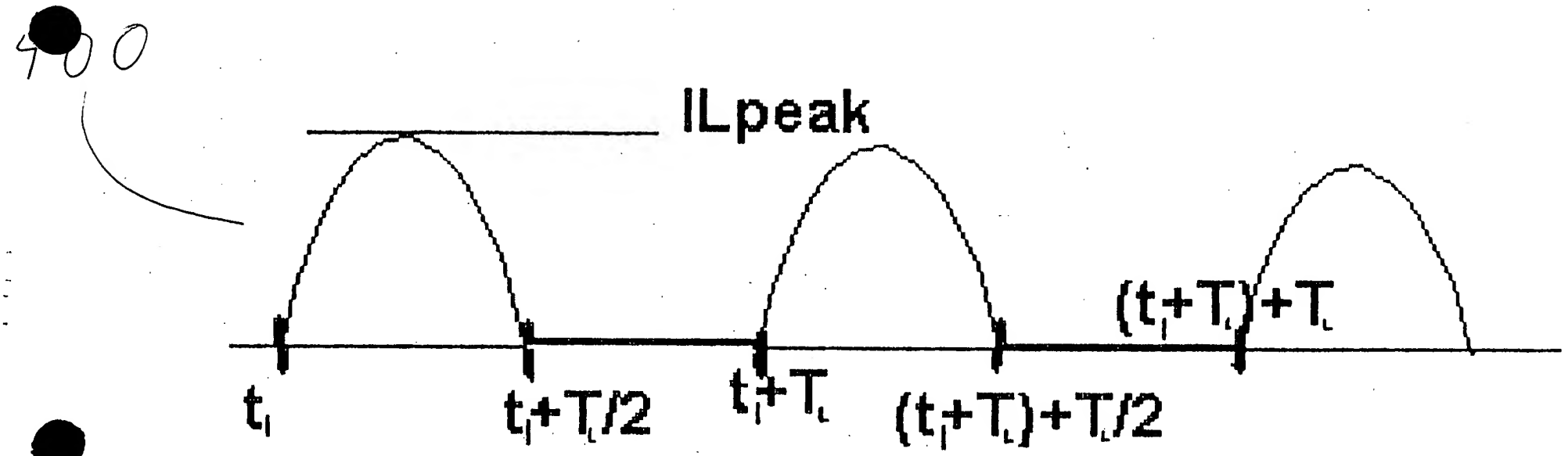


FIGURE 9a

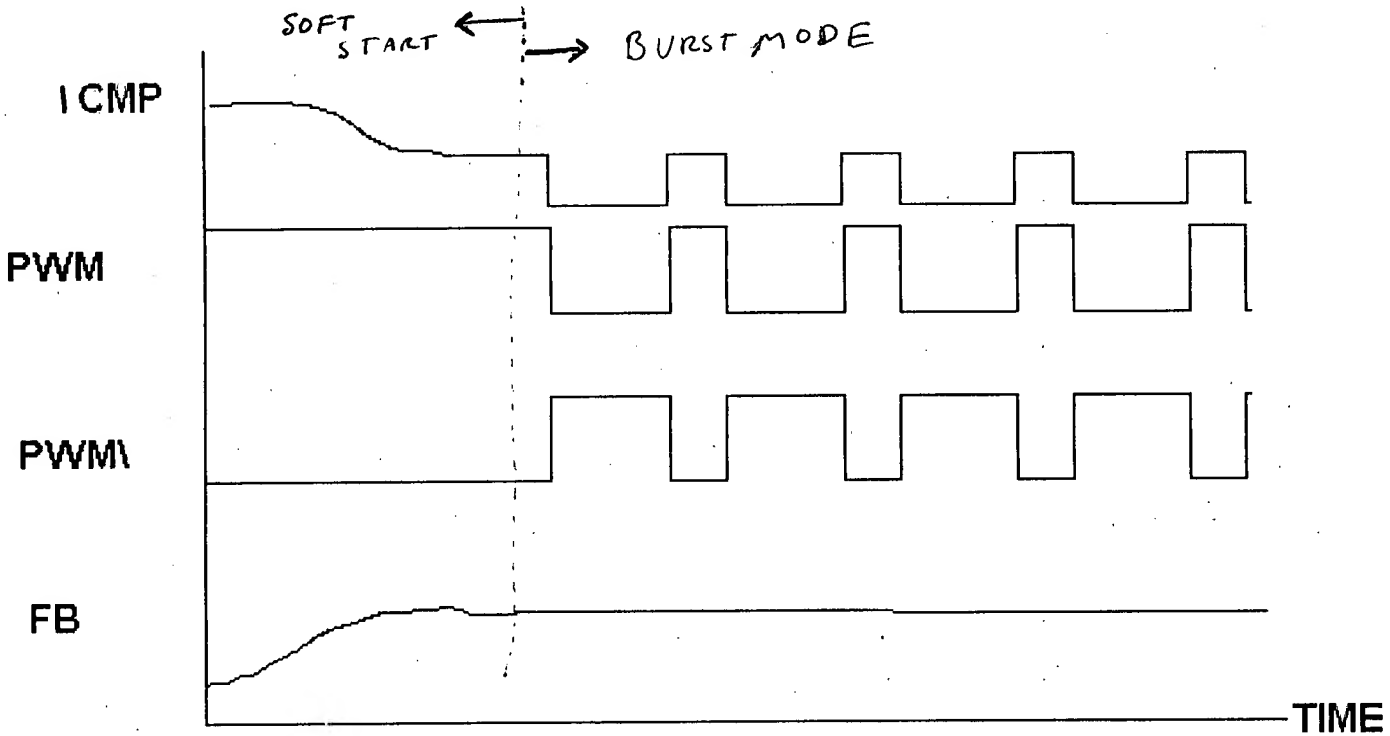


FIGURE 10

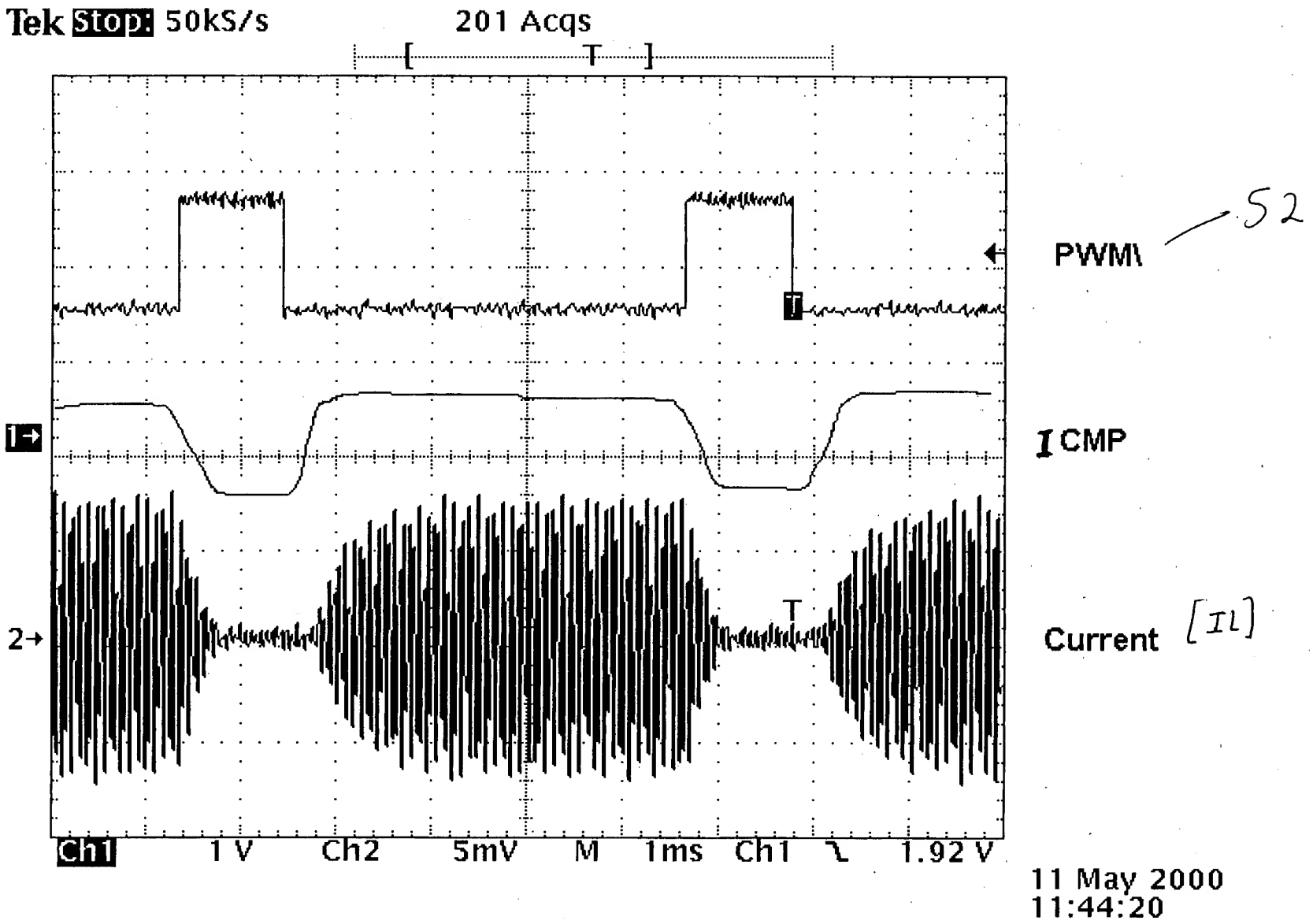

Tek Stop: 50kS/s
201 Acqs
PWM\
52
I CMP
Current [IL]
Ch1 1 V Ch2 5mV M 1ms Ch1 1.92 V
11 May 2000
11:44:20

FIGURE 11

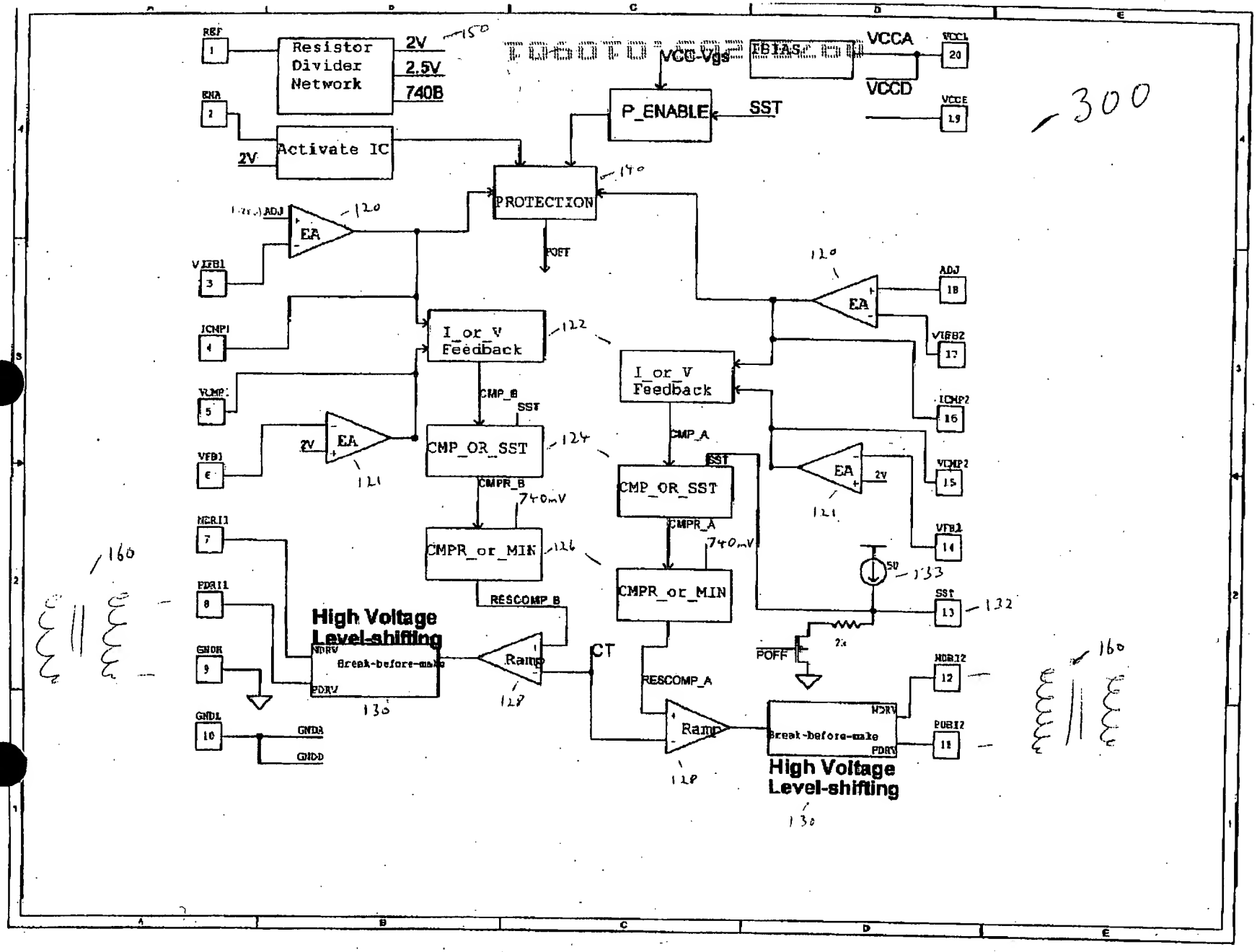

Resistor Divider Network
2V
2.5V
740B
Activate IC
P_ENABLE
SST
VCC-Vgs
BIAS
VCCA
VCCD
PROTECTION
EA
ADJ
VFB1
ICMP1
VCMP1
VFB1
I_or_V Feedback
CMP_B
CMP_OR_SST
CMPR_B
740mV
CMPR_or_MIN
RESCOMP_B
Ramp
CT
High Voltage Level-shifting
NDRV
PDRV
Break-before-make
NDRI1
PDRI1
GNDR
GNDL
GNDA
GNDD
I_or_V Feedback
CMP_A
CMP_OR_SST
CMPR_A
740mV
CMPR_or_MIN
RESCOMP_A
Ramp
POFF
SST
50
2x
ADJ
VFB2
ICMP2
VCMP2
VFB2
NDRI2
PDRI2
High Voltage Level-shifting
300
150
140
120
122
124
126
128
130
121
132
133
160

FIGURE 12

TO6070 S92S260

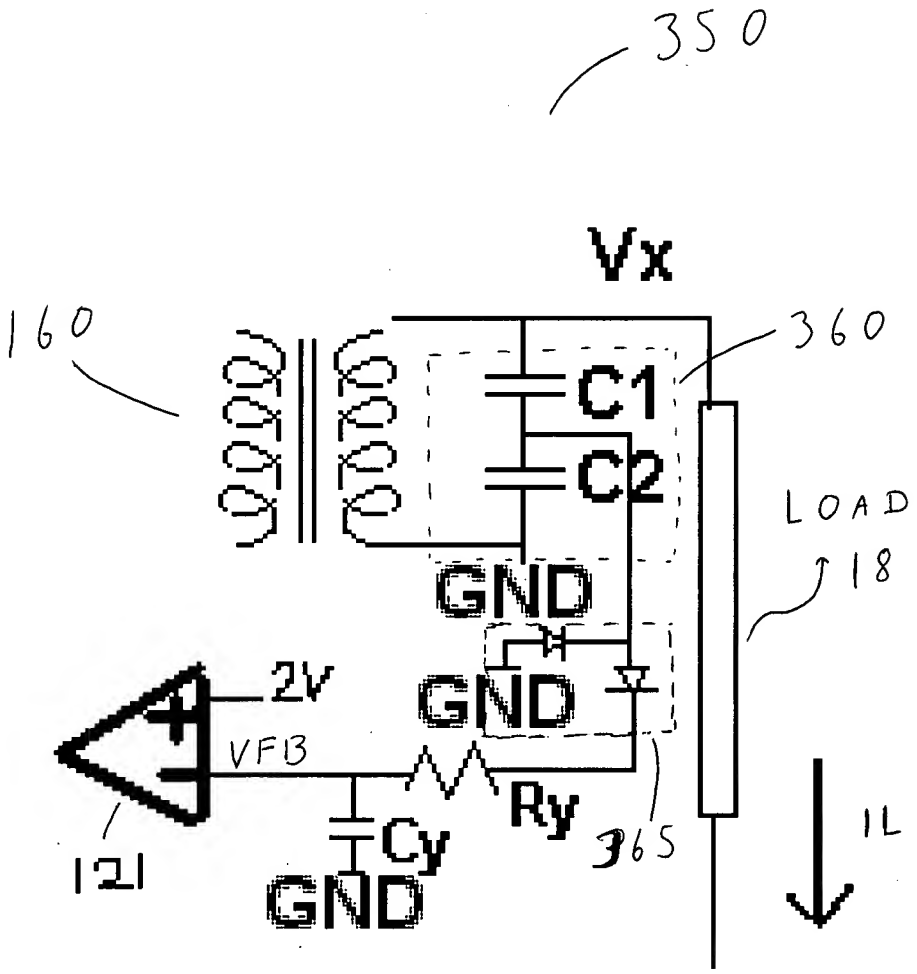
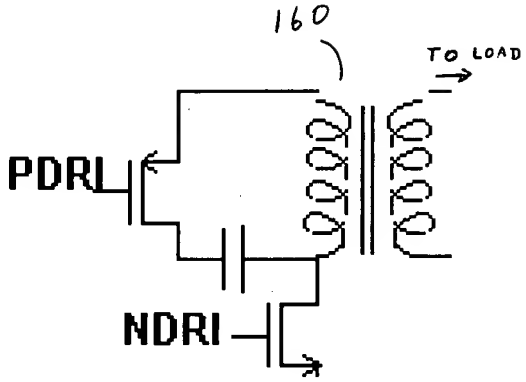
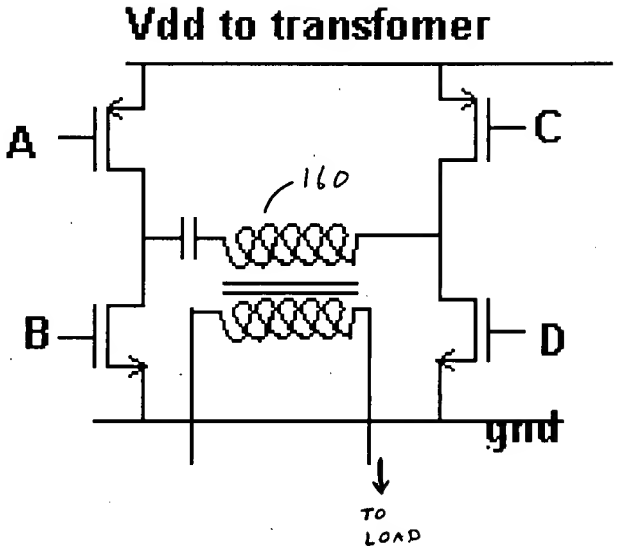


FIGURE 13



14(a)



14(b)

FIGURE 14

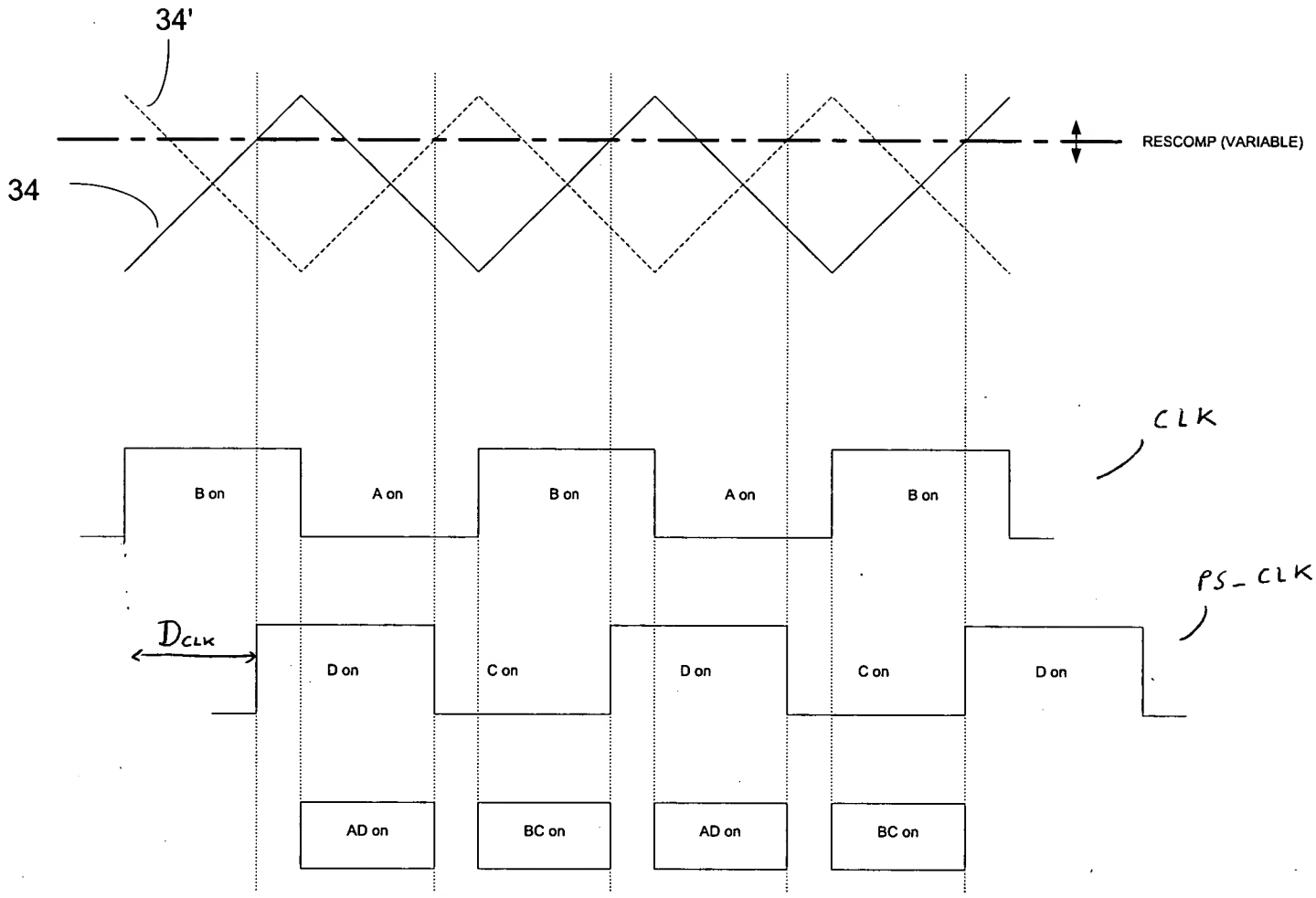

34'
34
RESCOMP (VARIABLE)
CLK
B on
A on
B on
A on
B on
PS_CLK
D_{CLK}
D on
C on
D on
C on
D on
AD on
BC on
AD on
BC on

FIGURE 15